A 17-GHz Direct Down-Conversion Mixer in a 47-GHz SiGe Process

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Abstract— **Future wireless data access will involve gigabit-per-second radios operating at RF frequencies above 10 GHz. This paper presents the design, simulation and measurement of a 17 GHz direct down-conversion mixer intended for these systems. The mixer was fabricated in a low-f_T (47 GHz) SiGe process, achieving a midband conversion gain of 12 dB and a double sideband noise figure of 11.5 dB, while consuming 17.8 mW from a 3.3 V supply.**

I. Introduction

The success of 2.5G cellular, and 802.11 WLANs has demonstrated that wireless data access is important to the public. 3G cellular and upcoming 802.11 standards will augment these services with higher data rates. However, these systems will still be limited to the 10's of megabits-per-second range and will remain a bottleneck for broadband networking.

A gigabit-per-second wireless solution is currently being developed by researchers at TRLabs [1]. The system operates at 17.35 GHz with a 400 MHz wide channel bandwidth. The design philosophy is to have a sophisticated base station and simple, low-cost, remote transceivers. This paper presents the design, simulation, and measurements of a direct down-conversion mixer targeted at this application.

Direct conversion has the potential for reduced power consumption, multi-band operation, reduced dependence on off-chip filters, higher levels of integration, and reduced system complexity. These are all design goals for the 17 GHz transceiver chip-set. However, direct conversion has four principle design challenges (DC offsets, even-order distortion, I/Q mismatches, and flicker noise) that must be considered during component and system design [2]-[3]. Also, for the gigabit-per-second application, overall radio performance is more dependent upon noise than linearity. Mixer design and performance results will be discussed in this context.

The mixer presented here is fabricated in IBM's SiGe 5HP BiCMOS technology with a relatively low cut-off frequency (f_T=47 GHz) [4] to achieve a low cost transceiver chip-set solution.

II. Mixer Cell Design Theory

As the second element in a direct conversion receiver, the mixer must have high conversion gain and low noise performance. An active mixer topology, based upon the standard Gilbert cell, was selected. The mixer core schematic is presented in Fig. 1. It consists of a transconductance pair Q1-Q2, a mixing quad Q3-Q6, loads R1-R2 and a resonant tank C_{tank}-L_{tank}.

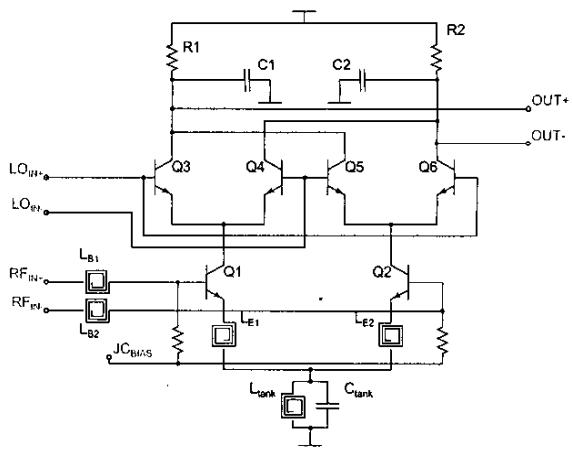

Fig. 1. Gilbert cell-based mixer core

The bases of the transconductance pair are the RF inputs to the mixer. In order to achieve a low noise figure and high conversion gain, the pair was simultaneously power and noise matched. The power matching condition requires that

$$Y_S = Y_{\text{in}}^*. \tag{1}$$

Conjugate matching of the input and source admittances allows maximum power transfer into the pair, thus increasing the mixer conversion gain. The input admittance

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Y_{in} depends on transistor bias and geometry, as well the emitter degeneration inductance L_E.

Noise matching involves matching the transconductance pair's optimum source admittance ($Y_{S_{\text{opt}}}$) to the admittance of the source (Y_S), or

$$Y_S = Y_{S_{\text{opt}}}. \tag{2}$$

When (2) is satisfied, the network's noise figure (NF) is minimized. NF_{min} can be further minimized by biasing the transconductance pair with its optimum collector current density ($J_{C_{\text{opt}}}$) [5].

Simultaneous power and noise matching thus involves satisfying the following:

$$Y_{S_{\text{OPT}}} = Y_{\text{in}}^*. \tag{3}$$

From the above relations a general strategy for the design of the transconductance pair was developed. The pair was first biased with its $J_{C_{\text{opt}}}$ to minimize NF_{min}. Next, transistor geometries and emitter inductances were scaled such that (3) was satisfied. The pair was then simultaneously noise and power matched to an arbitrary admittance. The system admittance of $\frac{1}{50\Omega}$ was then transformed into the arbitrary admittance with an "L"-match formed from the base inductor L_B and parasitic pad capacitance.

The mixing quad also has an important impact on mixer noise figure. Instances of imperfect switching, where both sides of a differential pair are on, will increase the mixer noise figure [6]. Therefore, the mixing quad transistors were sized smaller than those of the transconductance pair. This higher collector current density boosts the f_T for the quad transistors to the process maximum and gives improved switching performance.

Picohenry inductors L_B, L_E, and L_{tank} were designed and simulated using Ansoft HFSS. These inductors ranged in value from 75 to 262 pH. Because of reduced skin depths at 17 GHz, the inductor track widths could be decreased to reduce capacitance to the substrate and boost self-resonant frequencies. Also, minimal numbers of turns and side lengths were used to achieve quality factors of 10–15 at 17 GHz.

III. Additional Circuits

Additional circuits were included on-chip to facilitate single-ended testing. Shown in Fig. 2 are the LO buffer and baseband amplifier. The LO buffer is an active balun that converts the off-chip single-ended LO signal to a differential signal. Resistors R10-R11 provide a 400 mV_{p-p} (-4 dBm) LO signal to the mixing quad, while R9 provides level shifting.

The baseband amplifier is another active balun whose purpose is to take the differential mixer output and convert

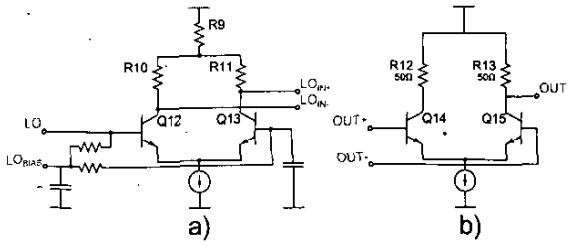

Fig. 2. a) LO Buffer b) baseband amplifier

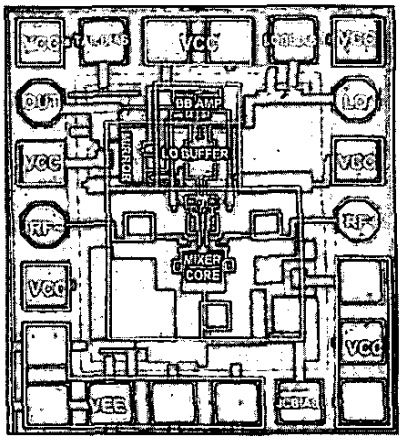

Fig. 3. Chip micro-photograph. (1060 μm x 910 μm)

it to a single-ended signal. In addition, the buffer provides approximately 3 dB of gain to the down-converted signal. Its outputs are matched to 50Ω. In order to facilitate DC-offset testing, the chip uses a negative supply voltage such that minimal current will be drawn through R13 during direct coupling to a 50Ω test load.

IV. Simulation and Measurements

The mixer was designed and simulated in Cadence SpectreRF and fabricated in IBM's SiGe 5HP process. The chip occupies 1060 μm x 910 μm as shown in Fig. 3. Measurements were performed using wire bonds for DC biases and wafer probes for RF signals.

The simulated and measured RF input match is shown Fig. 4. At 17.35 GHz the simulated and measured S_{11} are -13.5 dB and -10.5 dB respectively. The 3 dB discrepancy is attributed to differences in anticipated inductance for the bond wires and on-chip spiral inductors.

Excellent agreement is obtained between simulated and measured conversion gain, as shown in Fig. 5. The measured conversion gain of the circuit is 12 dB which includes 3 dB of gain from the on-chip baseband amplifier.

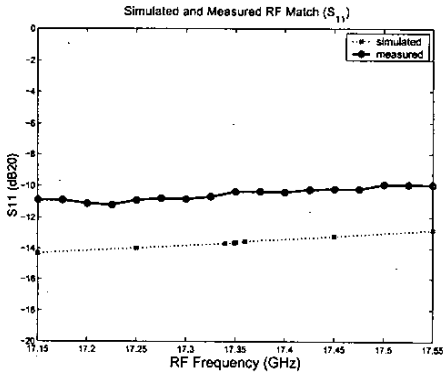

Fig. 4. Simulated and measured mixer RF input match

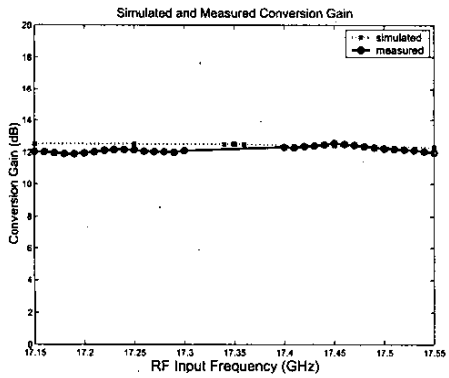

Fig. 5. Simulated and measured mixer conversion gain

Simulated and measured double-sideband noise figures are plotted in Fig. 6. Good agreement is obtained for frequencies in both the upper and lower sidebands. The measured double sideband noise figure is approximately 11.5 dB.

The simulated values for 1-dB compression point, IIP3 and IIP2 were -25 dBm, -13 dBm, and +30 dBm respectively. The corresponding measured values were P_{1dB} = -24 dBm, IIP3 = -10 dBm, and IIP2 = +21 dBm. Measured results for these tests are shown in Fig. 7 and 8. Although most tests were performed in a single-ended fashion, IIP2 was measured differentially. A differential RF input signal was constructed with a 90° phase splitter and two manually adjustable delay lines. The discrepancy between simulated and measured IIP2 is attributed to a high sensitivity of the manually tuned delay lines.

During differential testing, the DC-offsets at the output of the chip were measured and found to be less than 4 mV. The measured value for LO-to-RF leakage was -20 dB as compared to the simulated value of -26 dB.

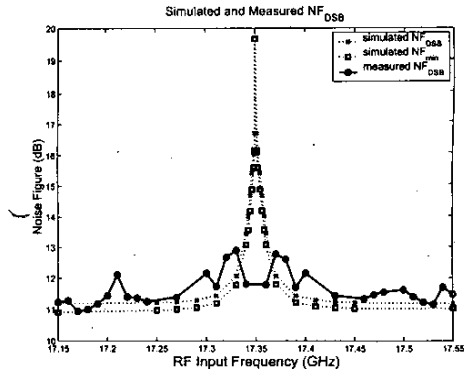

Fig. 6. Mixer double sideband noise figure

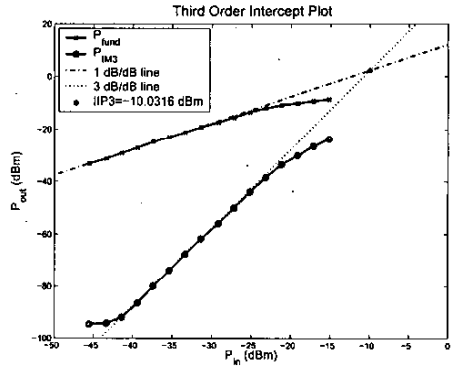

Fig. 7. Measured mixer third order intercept

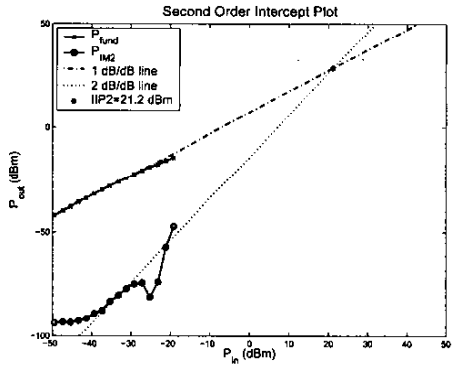

Fig. 8. Measured mixer second order intercept

Source	Technology	Frequency (GHz)	IF (GHz)	Gain (dB)	IIP3 (dBm)	Noise Figure DSB (dB)
[7]	SiGe (f_T=50 GHz)	11.2	1.25	16.1	.	9.4
[8]†	Si (f_T=52 GHz)	17.0	0.24	5.4	-9.9	8.8
[8]†	SiGe (f_T=80 GHz)	20.0	0.24	10.0	-11.3	6.0
[9]	SiGe (f_T=50 GHz)	20.0	1.00	10.0‡	-1.0	17.0
[10]†	SiGe (f_T=80 GHz)	30.0	0.30	5.9	.	10.0
This Work	SiGe (f_T=47 GHz)	17.35	0.00	12.0*	-10.0	11.5

† – utilizes off-chip inductive loads.

‡ – includes 8 dB of IF amplifier gain.

* – includes 3 dB of baseband amplifier gain.

TABLE I

COMPARISON WITH MIXERS FROM PREVIOUS WORKS

The mixer consumes 17.8 mW from a –3.3 V supply. The LO buffer and baseband amplifier consume 12.2 mW and 39.6 mW respectively. Table II summarizes the simulated and measured results.

	Simulated	Measured
RF frequency	17.35 GHz	
LO frequency	17.35 GHz	
LO power	-4 dBm	
Supply Voltage	-3.3 V	
Bias Current	5.4 mA	
RF match	-13.5 dB	-10.5 dB
Conversion Gain	12.5 dB	12 dB
NF_{DSB}	11.3 dB	11.5 dB
IP_{1dB}	-25 dBm	-24 dBm
IIP2	+30 dBm	+21 dBm
IIP3	-13 dBm	-10 dBm
LO-RF leakage	-26 dB	-20 dB
DC offset		< 4 mV

TABLE II

SUMMARY OF MEASURED RESULTS

Circuit performance is compared with previously published RFIC mixers operating above 10 GHz in Table I. Note that the present work features all components on-chip. As well, the majority of the 12 dB conversion gain arises within the mixer itself and not within baseband amplification circuits. The fully monolithic mixer presented here achieves very good 17 GHz performance with a relatively low-f_T (47 GHz) process.

V. CONCLUSION

The design, simulation and measured results for a 17 GHz direct down-conversion mixer were presented. The mixer was designed to be simultaneously noise and power matched so as to achieve optimum performance in a direct conversion receiver. The circuit achieved a midband conversion gain of 12 dB and a double sideband noise figure of 11.5 dB. These results demonstrate that successful RFIC design using low f_T SiGe processes can be performed at 17 GHz and above.

ACKNOWLEDGMENTS

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